AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 1 and 11 and add new claims 13 and 14 as follows:

LISTING OF CLAIMS:

1. (Currently Amended) A leakage current reducing method of an LSI for reducing leakage current in an LSI chip divided into two parts; namely a main power supply region including circuits operated by receiving power from a main power source, and a backup power supply region including circuits operated by receiving power from a backup power source, said LSI chip having a scanning control circuit and a power supply cut-off controller built-in to the LSI chip, said method comprising the steps of:

connecting memory units in each of the circuits provided in the main power supply region through a scan path;

starting a scanning operation, when the LSI chip is placed in an operation standby state, through the scan path, and reading information held in the memory units of each of the circuits provided in the main power supply region based upon a scan mode signal and a scanning clock pulse; and

saving the information thus read by the scanning operation in a built-in storage section provided in the backup power supply region.

2. (Original) The leakage current reducing method according to claim 1, wherein said built-in storage section is formed by an SRAM.

3. (Original) The leakage current reducing method according to claim 1, wherein said step of saving is conducted into a scanned information storage section which is separately provided from said built-in storage section, in a case where said built-in storage section is used for a normal operation.

4. (Original) The leakage current reducing method according to claim 3, wherein said scanned information storage section is formed by an SRAM.

5. (Original) The leakage current reducing method according to claim 3, wherein a scan path originally prepared for testing the LSI chip is used as the scan path for reading information held in the memory units of each of the circuits provided in the main power supply region.

6. (Original) The leakage current reducing method according to claim 1, wherein a part of said built-in storage section provided in the back up power supply region is used as a scanned information storage portion for storing the information read by the scanning operation, said method comprising the steps of:

starting the scanning operation, when the LSI chip is placed in the standby state, through the scan path, serially reading the information held in the memory units of each of the circuits provided in the main power supply region, converting the read serial information into parallel information, and saving the thus converted parallel information in specified addresses of the scanned information storage portion of the built-in storage section; and

parallely reading, when the LSI chip is returned from the standby state, the information held in the scanned information storage portion of the built-in storage section by specifying addresses therefor, converting the read parallel information into serial information, and setting the serial information through the scan path in the memory units of each of the circuits provided in the main power supply region.

7. (Original) The leakage current reducing method according to claim 3, wherein said built-in storage section and said scanned information storage section are each formed by an SRAM.

8. (Original) The leakage current reducing method according to claim 1 comprising a step of increasing a substrate bias voltage of a transistor of each of the circuits provided in the backup power supply region while the LSI chip is in the operation standby state.

9. (Original) The leakage current reducing method according to claim 1, comprising the steps of:

presetting a voltage of the backup power source to be lower than a voltage of the main power source, yet enough for holding the content of the storage section provided in the backup power supply region; and

supplying power to the backup power supply region from the main power source in a normal operation state, and from the backup power source in an operation standby state.

10. (Previously Presented) The leakage current reducing method according to claim 3, wherein said built-in storage section is formed by an SRAM.

11. (Currently Amended) A leakage current reducing method of an LSI for reducing leakage current in an LSI chip divided into two parts; namely a main power supply region including circuits operated by receiving power from a main power source, and a backup power supply region including circuits operated by receiving power from a backup power source, said LSI chip having a scanning control circuit and a power supply cut-off controller built-in to the LSI chip, said method comprising the steps of:

disposing an external storage section operated by receiving power from the backup power source outside the LSI chip, and connecting memory units of each of the circuits provided in the main power supply region through a scan path;

starting a scanning operation, when the LSI chip is placed in an operation standby state, through the scan path, serially reading information held in the memory units of each of the circuits provided in the main power supply region based upon a scan mode signal and a scanning clock pulse, converting the read serial information into parallel information, and then saving the parallel information in the external storage section by specifying addresses therefor; and

parallely reading, when the LSI chip is returned from the standby state, the information held in the external storage section by specifying addresses therefor, converting the read parallel information into serial information, and then setting the serial information in the memory units of each of the circuits provided in the main power supply region through the scan path.

12. (Original) The leakage current reducing method according to claim 11, wherein a part of said external storage section is used as a scanned information storage section for storing the information read by the scanning operation.

13. (New) The leakage current reducing method according to claim 1, wherein the scanning control circuit generating the scan mode signal and scanning clock pulse.

14. (New) The leakage current reducing method according to claim 11, wherein the scanning control circuit generating the scan mode signal and scanning clock pulse.